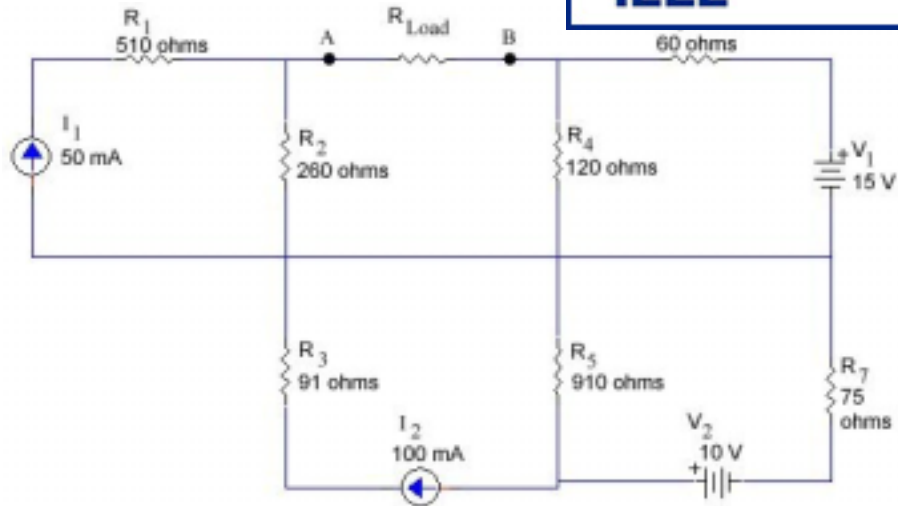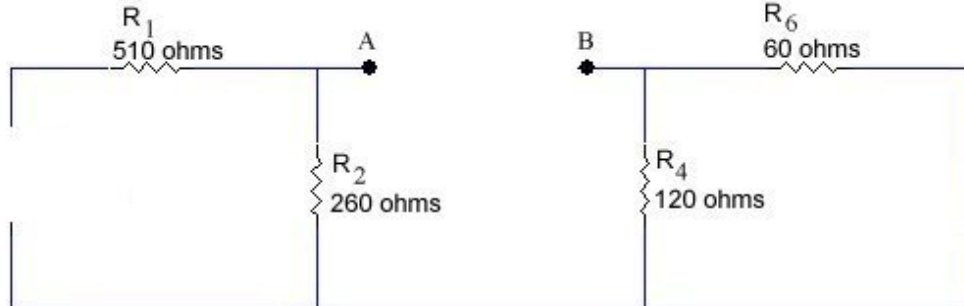1)

Figure 1

a) Determine and sketch the Thevenin's equivalent circuit for the output terminals A and B.
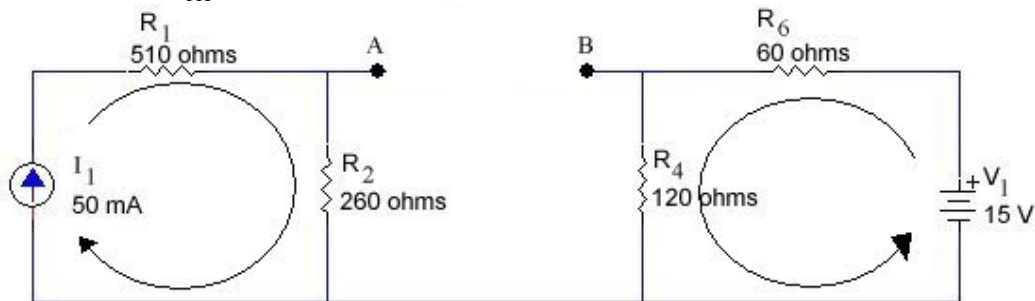
Solution

First one should realize that R_3, R_5, and R_7 along with I_2 and V_2 have no bearing on the final solution. Thus the circuit to determine R_{TH} is:

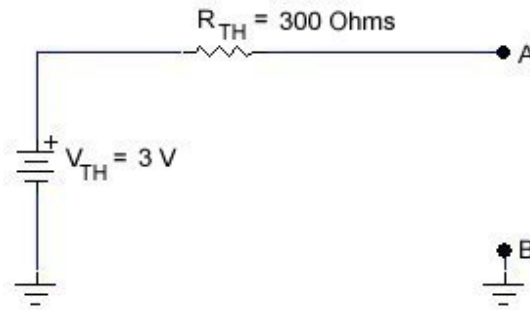$R_{TH} = R2 + R4//R6 = 300\Omega$

Circuit to determine V_{TH} is:

$V_A = I_1 \times R_2 = 50 \text{ mA} \times 260\ \Omega = 13 \text{ V}$ and $V_B = V_1 \dfrac{R_4}{R_4 + R_6} = 15V \dfrac{120\Omega}{120\Omega + 60\Omega} = 10V$

$V_{AB} = V_{TH} = V_A - V_B = 13 \text{ V} - 10 \text{ V} = 3 \text{ V}$

Thevenin Equivalent Circuit.

b) At what value of load resistance will 600 µA flow through the load?

$$R_{Load} = \underline{\quad 4.7 \text{ k}\Omega \quad}$$

$$600\mu A = \frac{V_{TH}}{R_{TH} + R_{Load}} \quad \therefore R_{Load} = \frac{V_{TH}}{600\mu A} - R_{TH} = \frac{3V}{600\mu A} - 300\Omega = 4.7k\Omega$$

c) At what value of load resistance is maximum power transferred?

$$R_{Load} = \underline{\quad 300 \ \Omega \quad}$$

Maximum Power is transferred when $R_{Load} = R_{TH} = 300 \ \Omega$

d) What would be the minimum load resistance if this Thevenin's equivalent circuit was to be a stiff voltage supply?
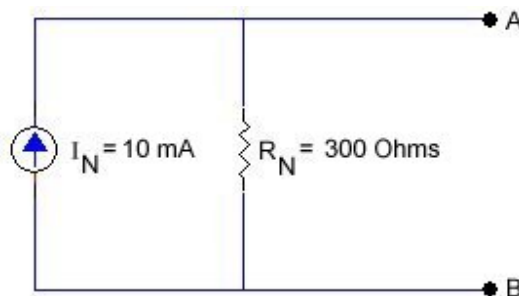
$$R_{Load(min)} = \underline{\quad 30 \text{ k}\Omega \quad}$$

From the definition of a stiff supply! $R_{Load(min)} = 100 \times R_S$. In this case R_S is the Thevenin resistance (R_{TH}). Hence $R_{Load(min)} = 100 \times 300 \ \Omega = 30 \text{ k}\Omega$

e) What is the Norton's equivalent circuit?
    (Provide a circuit sketch as well)

$R_N = R_{TH} = 300 \ \Omega$ and $I_N = \dfrac{V_{TH}}{R_{TH}} = \dfrac{3V}{300\Omega} = 10mA$

Norton Equivalent
Circuit.

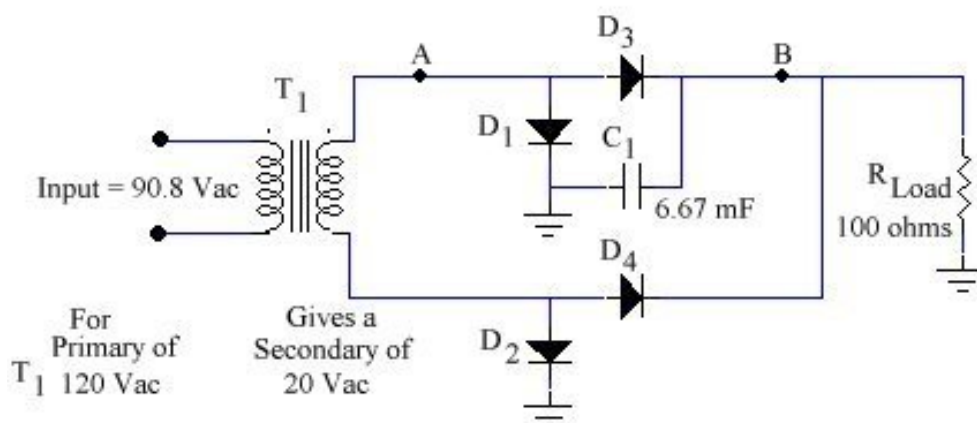2) **(Use the second approximation of the diode!)**

Figure 2

NOTE: There is an error on the diagram, both D_1 and D_2 should be flipped so that the anode is connected to ground. With the above configuration the output would be zero as there is no ground connection for current flow.

a) What is the peak or maximum voltage across the load?

$$V_{Load} = \underline{\quad 20 \text{ V} \quad}$$

For a primary transformer voltage of 120 Vac gives a secondary voltage of 20 Vac means that the transformer turns ratio is, $\dfrac{120Vac}{20Vac} = 6$. Thus for a primary voltage of 90.8 Vac the secondary voltage is $\dfrac{90.8Vac}{6} = 15.133Vac = 15.133Vac \times \sqrt{2} \cong 21.4V_P$

Realizing that this is a bridge rectifier and the fact that we are using the second approximation of the diode gives a load voltage of 21.4 V – 1.4 V = 20 V.

b) What is the peak to peak ripple voltage at the load?

$$V_{ripple} = \underline{\quad 0.250 \text{ V}_{P\text{-}P} \quad}$$

$I_{Load(max)} = \dfrac{V_{Load}}{R_{Load}} = 0.2A$ and since this is a bridge rectifier circuit as well means that the rectified frequency is double the input frequency of 60 Hz. Hence the time between charging for the capacitor is $\dfrac{1}{120Hz} = 8.\overline{3}m\sec$

So to find the change in charge is as follows; $\quad \Delta Q = 0.2A \times 8.\overline{3}m\sec = 1.\overline{6}mC$

$\text{Capacitance} = \dfrac{\Delta Q}{\Delta V} \therefore \Delta V = \dfrac{\Delta Q}{C} = \dfrac{1.\overline{6}mC}{6.67mF} = 249.9mV_{P-P} \cong 0.250V_{P-P}$

c) What rectifier configuration is this supply? **Bridge Rectifier (well supposed to be 🌀)**
d) Using the graph on the next page, sketch the waveform at point 'A'. Also on the same graph
sketch the resulting waveform at point 'B' both with and without the capacitor in circuit.
(You must indicate which waveform is which along with voltage levels.)
Please try to be neat! A sloppy diagram may lead to a misinterpretation and lost marks.
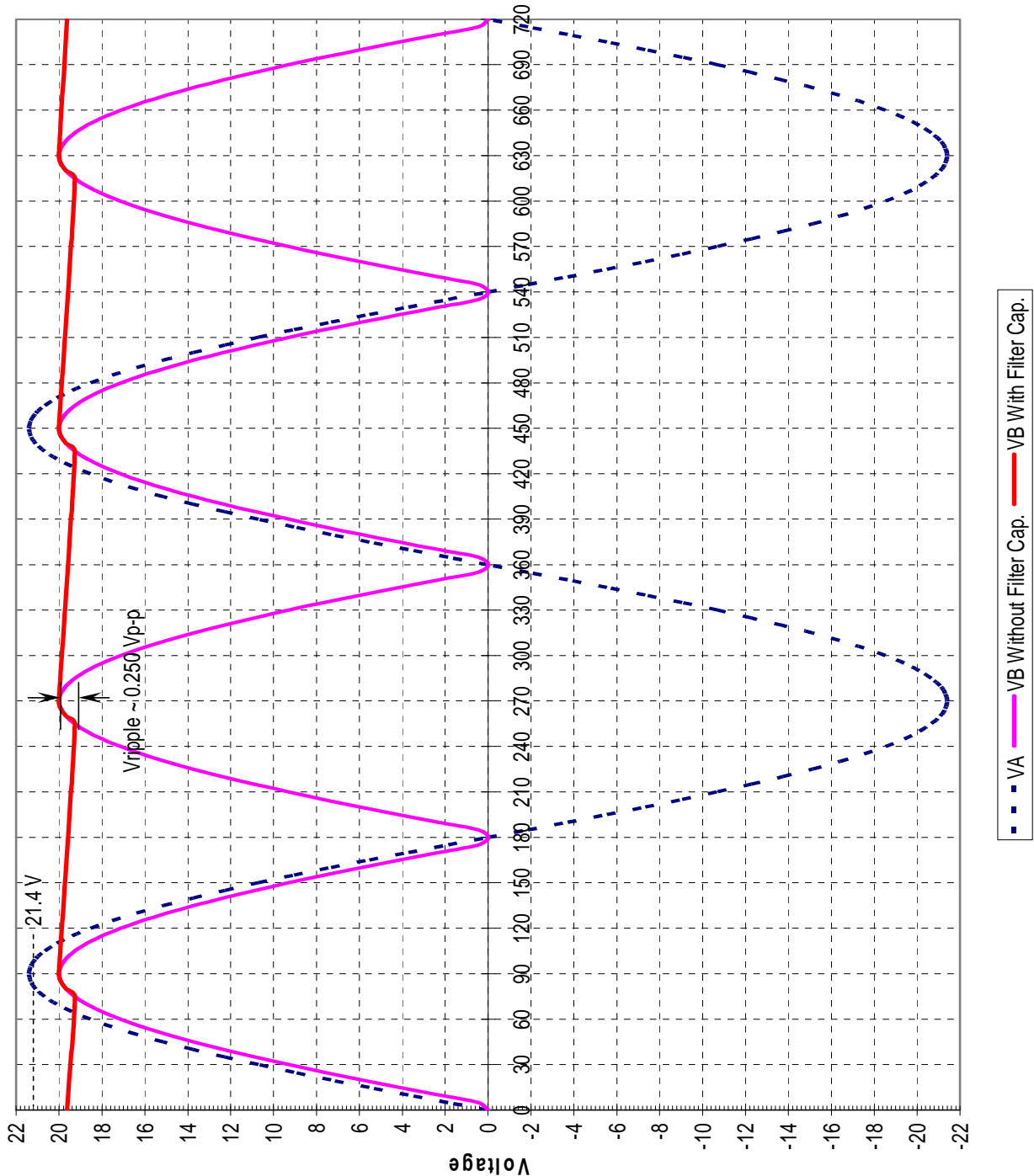
3) **(Use the second approximation of the diode!)**
Sketch the waveform at each terminal, A, B, C, and D on the supplied graphs.

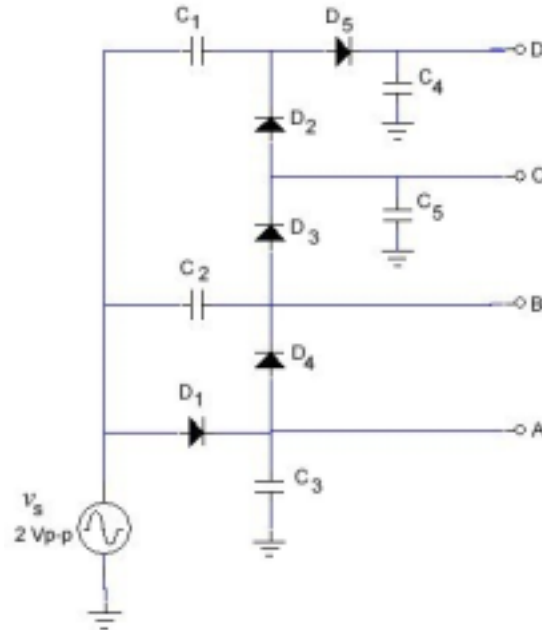**Please try to be neat! A sloppy diagram may lead to a misinterpretation and lost marks.**

Figure 3

Circuit break down:
D_1 and C_3 = Peak Detector 1. Sets up a bias for Clamper 1.

C_2 and D_4 = Clamper 1.

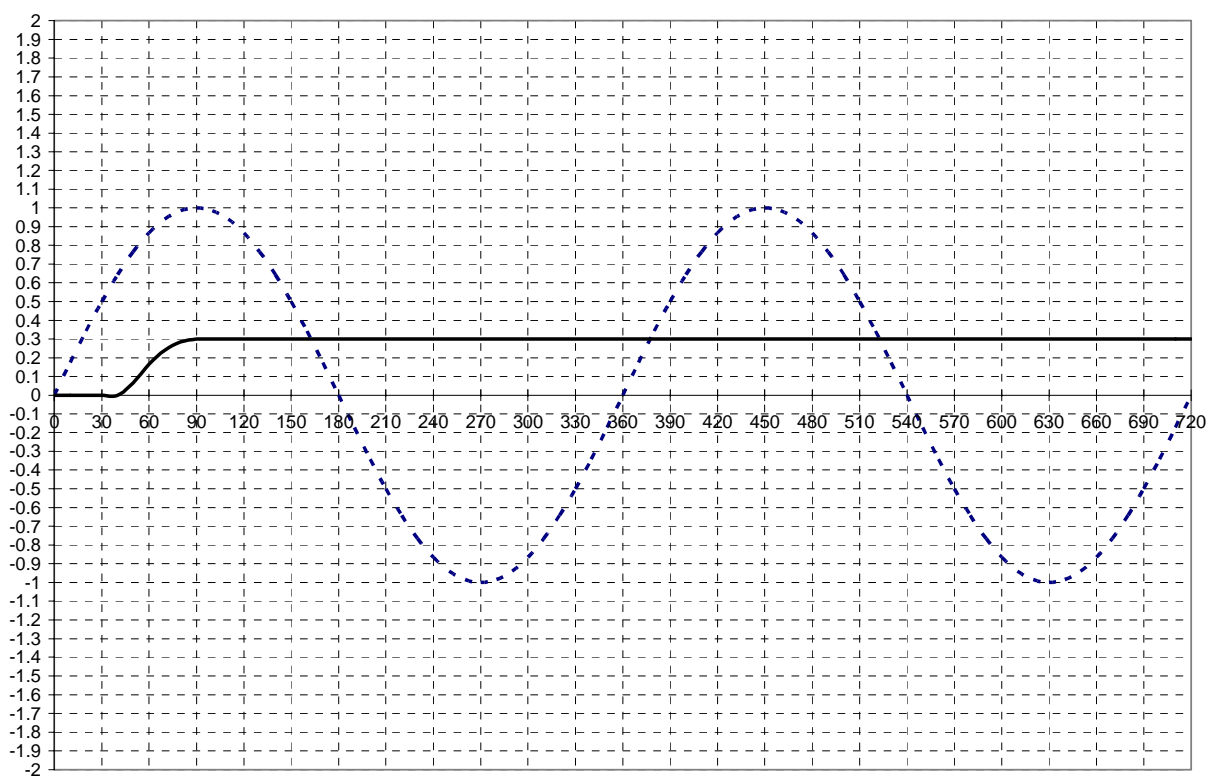D_3 and C_5 = Peak Detector 2. Sets up a bias for Clamper 2.

C_1 and D_2 = Clamper 2.
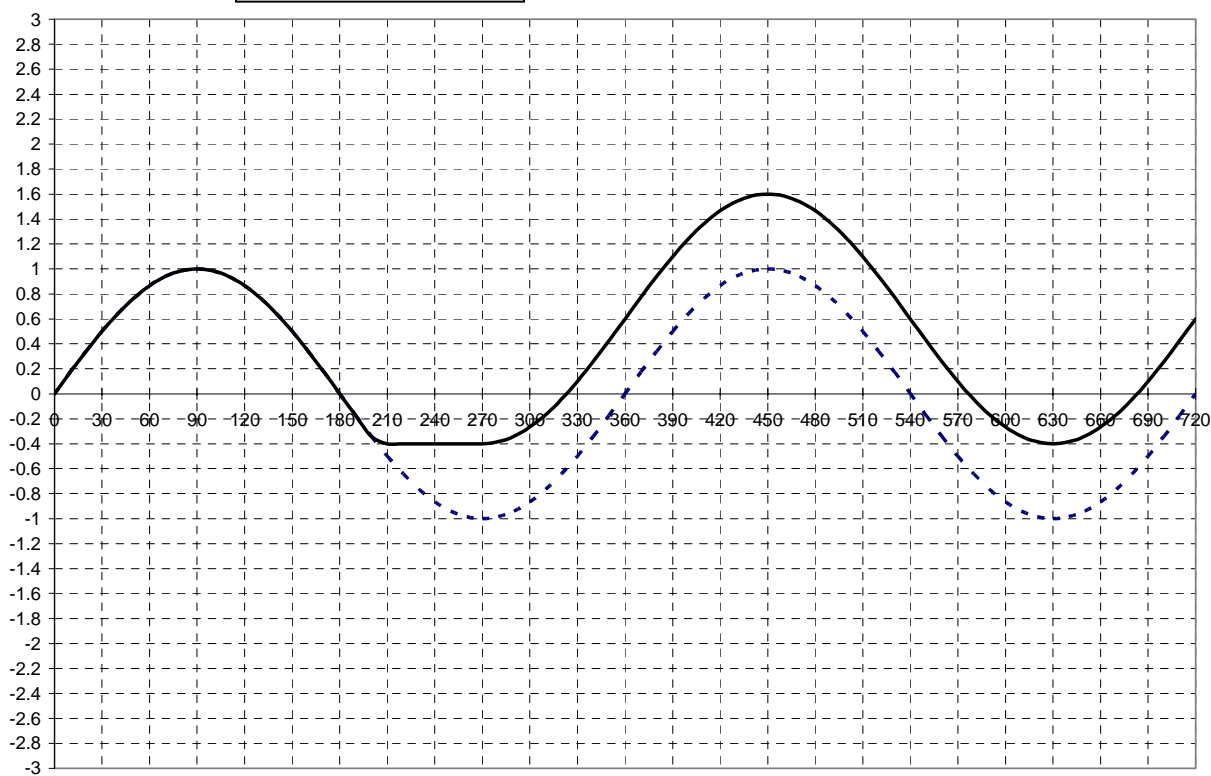
D_5 and C_4 = Peak Detector 3.

Question 3 Continued

Graph 1 for V_A - - - Vs ——— VA

Graph 2 for V_B - - - Vs ——— VB

Question 3 Continued
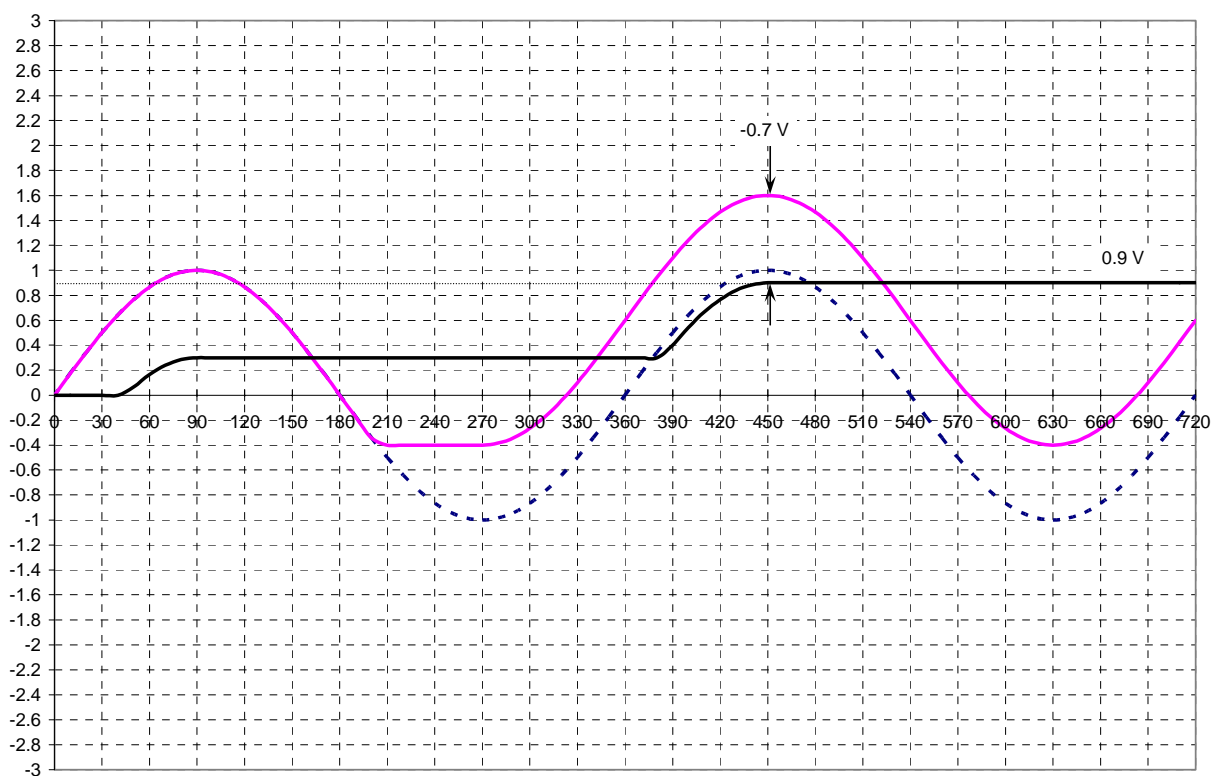
Graph 3 for V_C

Vs ----- VB ——— VC
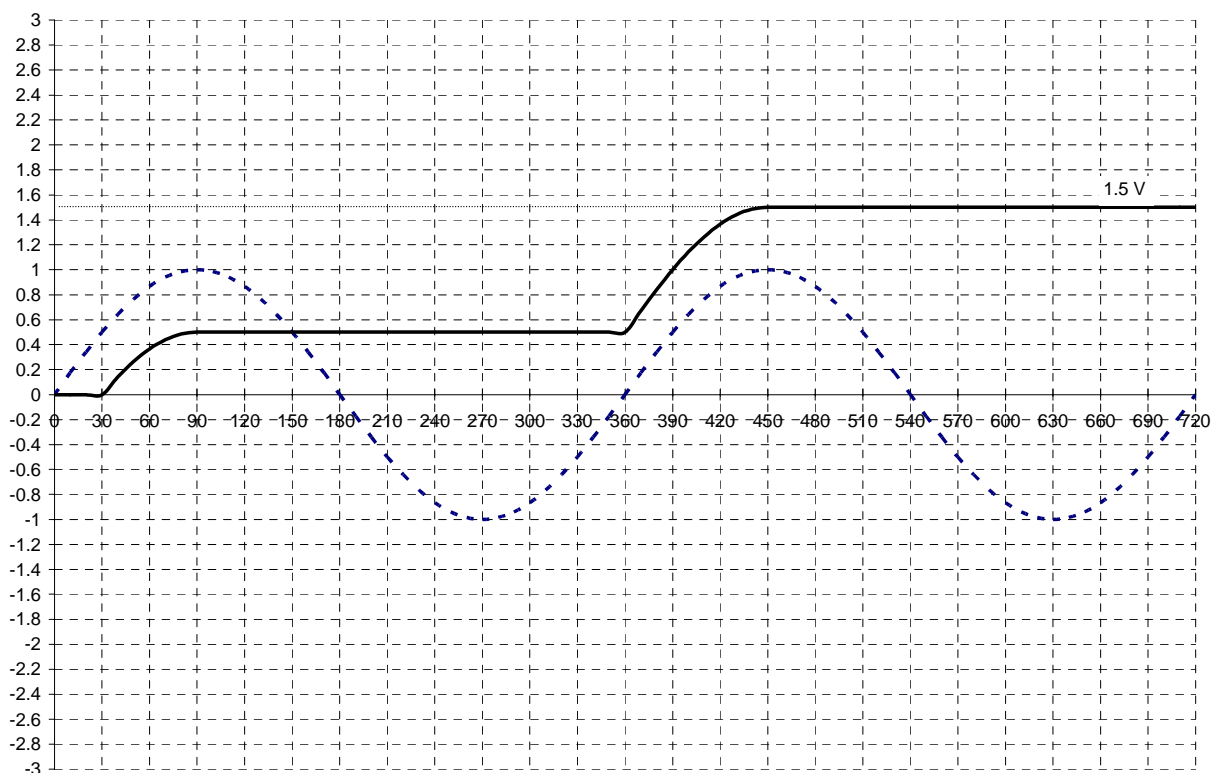
Graph 4 for V_D

Vs ----- VD

4) **(Use the second approximation of the diode!)**
With the given V_{in} sketch V_{out} on the same graph.

Please try to be neat! A sloppy diagram may lead to a misinterpretation and lost marks.

Because there are supplies attached means that the diodes will have a forward biased region for an input waveform. To determine what this region is and how the output will look is as follows. First let's determine a relationship between Vin and Vout. This can be done by choosing an intermediate point such as V_1.

$V_{out} = V_1 + 0.7$ V and $V_1 = V_{in} – 0.7$ V

→ $V_{out} = V_{in} – \cancel{0.7\ V} + \cancel{0.7\ V}$

But this is not for all cases of Vin! The upper end will be limited by the +4 V supply. In other words for an input signal greater than 4 V D_2 will be reversed biased. To determine the lower limit we have to find what V_1 is when no input signal is applied. In this condition current will flow from the +4 V supply through R_2, D_2 and R_1 to the –2 V supply.

+4 V

R_2 1 kohm

D_1 D_2 V_{out}
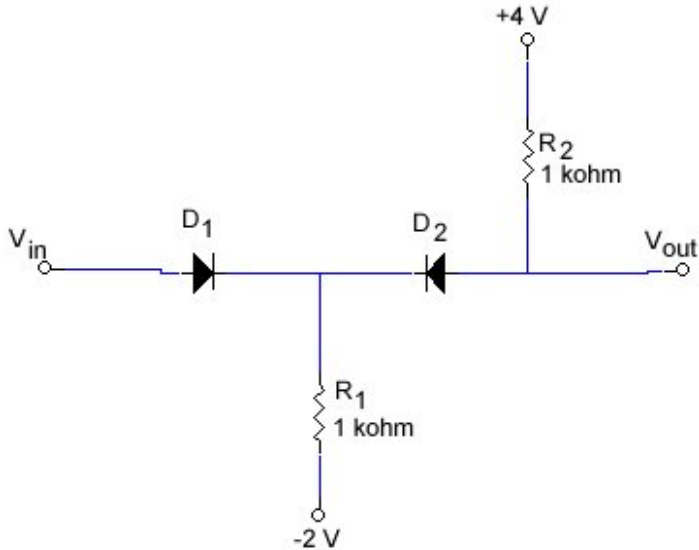
V_{in}

R_1 1 kohm

-2 V

Figure 4

$$I = \frac{4V - 0.7V - (-2V)}{R_1 + R_2} = 2.65mA$$

$$V_1 = IR_1 - 2V = 0.65V$$

But we are interested in $V_{out} = V_1 + 0.7$ V = 1.35 V therefore the lower limit is 1.35 V.

1.35 V

Vin — Vout
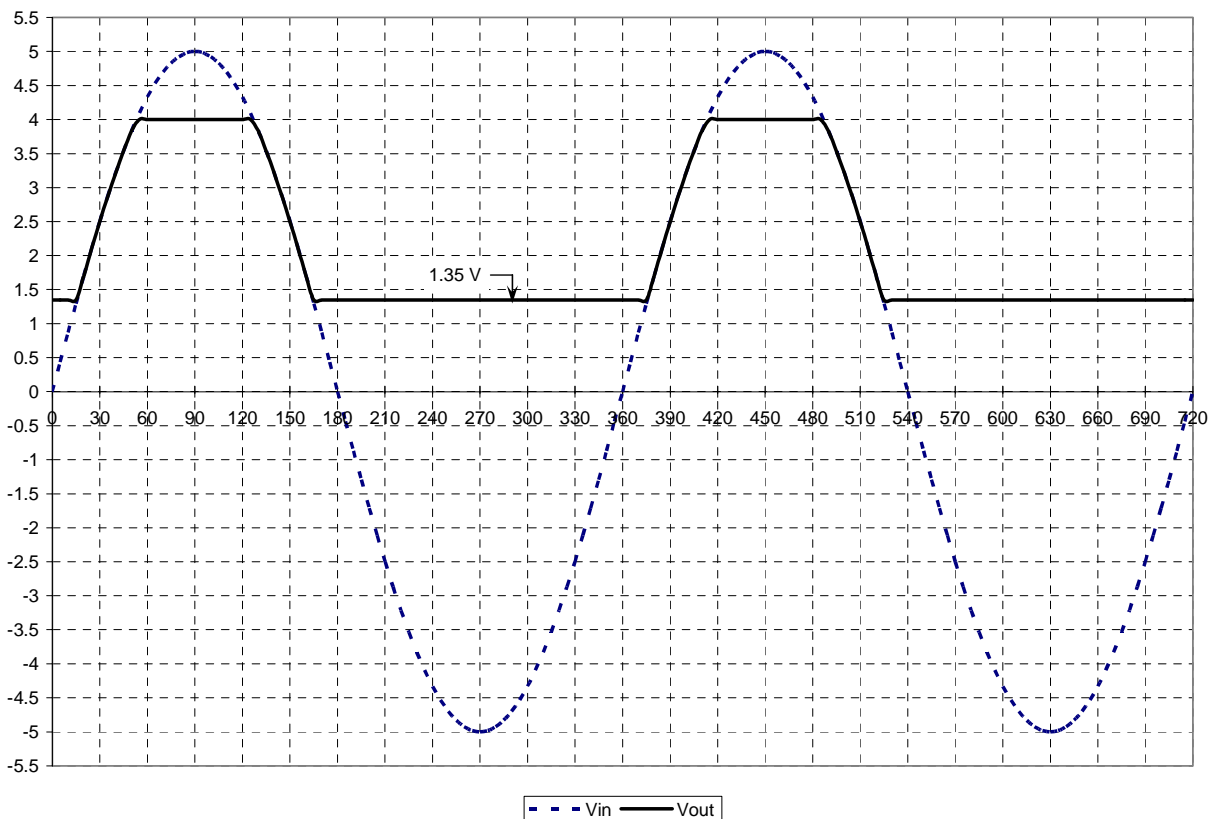
5)   (Assume $\beta = 100$, $V_{BE} = 0.7$ V and $V_{CE(sat)} = 0.3$ V)

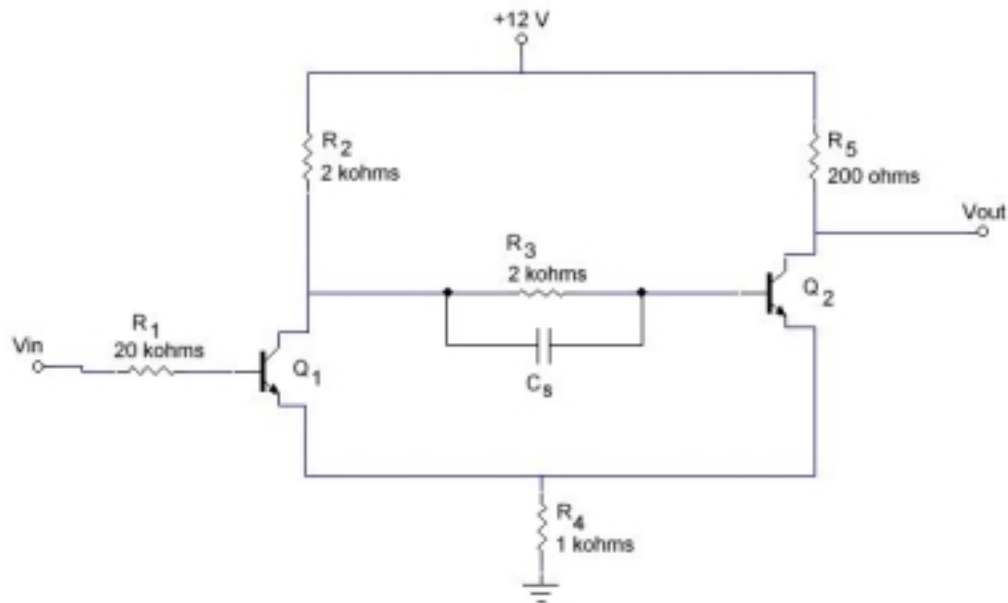**Figure 5**

Find the following for the above transistor Schmitt trigger.
a) Determine the:

- Upper Trip Point? UTP = __10 V__

- Lower Trip Point? LTP = __4 V__

- Hysteresis Voltage? V_H = __6 V__

$$UTP = \frac{R_4}{R_4 + R_5} V_{CC} = \frac{1k\Omega}{1k\Omega + 200\Omega} 12V = 10V$$

$$LTP = \frac{R_4}{R_2 + R_4} V_{CC} = \frac{1k\Omega}{2k\Omega + 1k\Omega} 12V = 4V$$

$$V_H = UTP - LTP = 10V - 4V = 6V$$

Question 5 Continued

b) It is determined that a capacitor can be used in order to increase the switching time.
On the circuit diagram sketch where this capacitor is to be connected.
See C_S on diagram (Figure 5)!

c) If this was a 621 pF capacitor, what would the maximum switching frequency be?

$$F_{max} = \underline{\ 700\ kHz\ }$$

$$C = \frac{t_{re}}{2.3R} \quad tre = \frac{1}{F_{max}} \quad R = R_3 // R_2 \quad \therefore C = \frac{\dfrac{1}{F_{max}}}{\dfrac{2.3R_2 R_3}{R_2 + R_3}} = \frac{R_2 + R_3}{2.3R_2 R_3 F_{max}}$$

$$\Rightarrow F_{max} = \frac{R_2 + R_3}{2.3R_2 R_3 C} = \frac{2k\Omega + 2k\Omega}{2.3 \times 2k\Omega \times 2k\Omega \times 621pF} = 700.13kHz \cong 700kHz$$

d) List two advantages the transistor Schmitt Trigger has over a Basic Transistor Switch.

1) Different trip points for turn on (UTP) and turn off (LTP).

2) The output signal tracks the input signal. i.e. When the input is low the output is low and when the input is high the output is high.

6)   (Assume $\beta = 100$, $V_{BE} = 0.7$ V, $V_{CE(sat)} = 0.3$ V, and at room temperature (300 $^{\circ}$K))
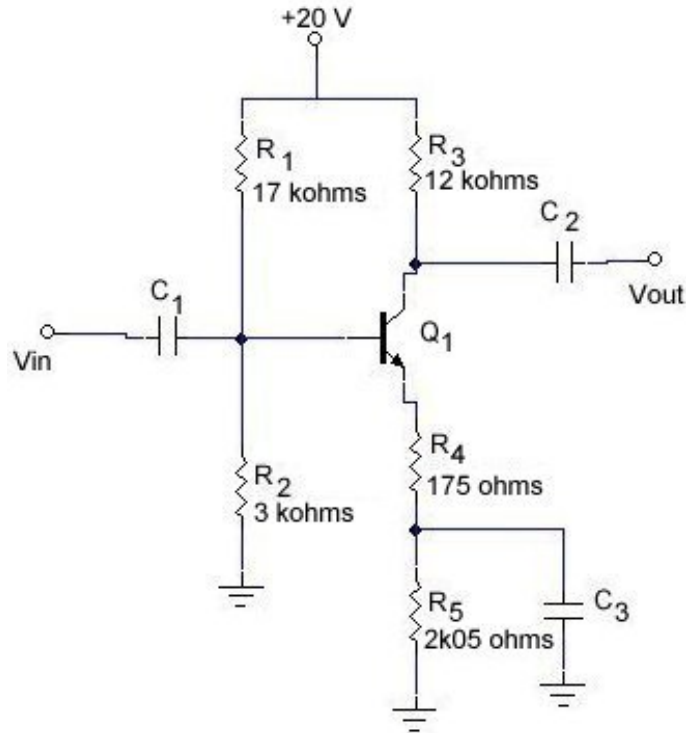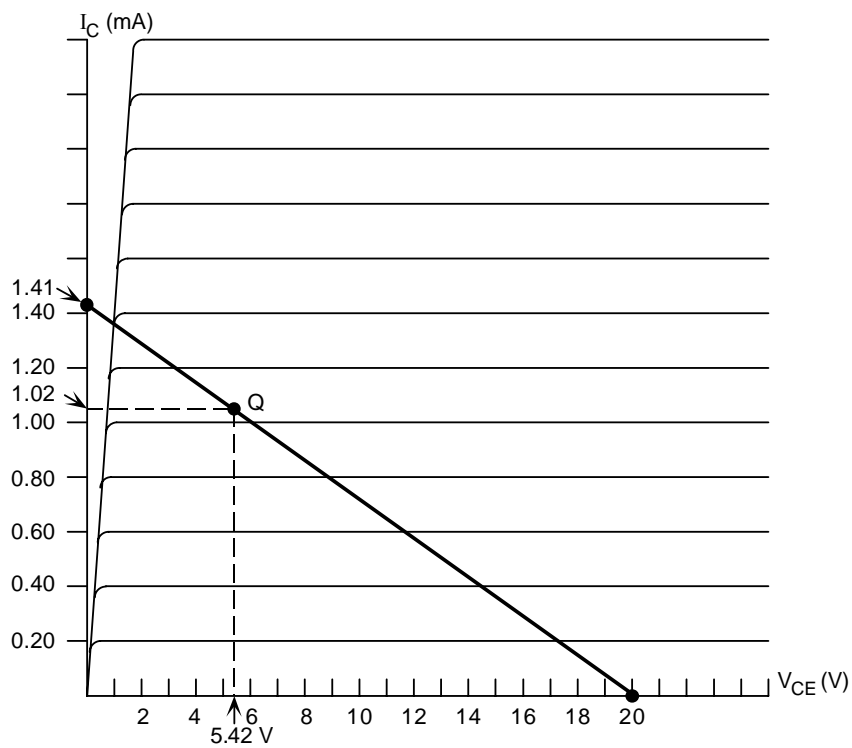

Figure 6

a) Draw the DC load line and determine the Q point.
   (Use the supplied transistor curve and label the X and Y axis' values)

$I_{CQ} = \underline{\ 1.02\ mA\ }$ $V_{CEQ} = \underline{\ 5.42\ V\ }$

Question 6 Continued
Page for Q point calculations

$$I_{C(\max)} = \frac{V_{CC}}{R_3 + R_4 + R_5} = \frac{20V}{12k\Omega + 175\Omega + 2.05k\Omega} = 1.406mA \cong 1.41mA$$

$$V_{BQ} = V_{CC} \frac{R_2}{R_1 + R_2} = 20V \frac{3k\Omega}{17k\Omega + 3k\Omega} = 3V$$

$$V_{EQ} = V_{BQ} - V_{BE} = 3V - 0.7V = 2.3V$$

$$I_{EQ} = \frac{V_{EQ}}{R_4 + R_5} = \frac{2.3V}{175\Omega + 2.05k\Omega} = 1.034mA$$

$$I_{CQ} = \frac{\beta}{\beta + 1} I_{EQ} = \frac{100}{100 + 1} 1.034mA = 1.024mA \cong 1.02mA$$

$$V_{CQ} = V_{CC} - I_{CQ}R_3 = 20V - 1.024mA \times 12k\Omega = 7.72V$$

$$V_{CEQ} = V_{CQ} - V_{EQ} = 7.72V - 2.3V = 5.42V$$

Question 6 Continued

b) Determine the input impedance (Zin), output impedance (Zout) and voltage gain (Av).

$$Zin = \underline{\quad 2.26 \text{ k}\Omega \quad} \qquad Zout = \underline{\quad 12 \text{ k}\Omega \quad} \qquad Av = \underline{\quad \text{- 60} \quad}$$

$$Z_{out} = R_3 = 12k\Omega$$

$$Z_{in} = R_1 // R_2 // \beta(r'e + R_4)$$

$$r'e = \frac{V_T}{I_{EQ}} \qquad V_T = \frac{kT}{q} = 0.02585V \text{ @ room temp. (300°K). } \therefore r'e = \frac{0.02585V}{1.034mA} \cong 25\Omega$$

$$Z_{in} = 17\ k\Omega // 3\ k\Omega // 100(25\ \Omega + 175\ \Omega) = 2.26\ k\Omega$$

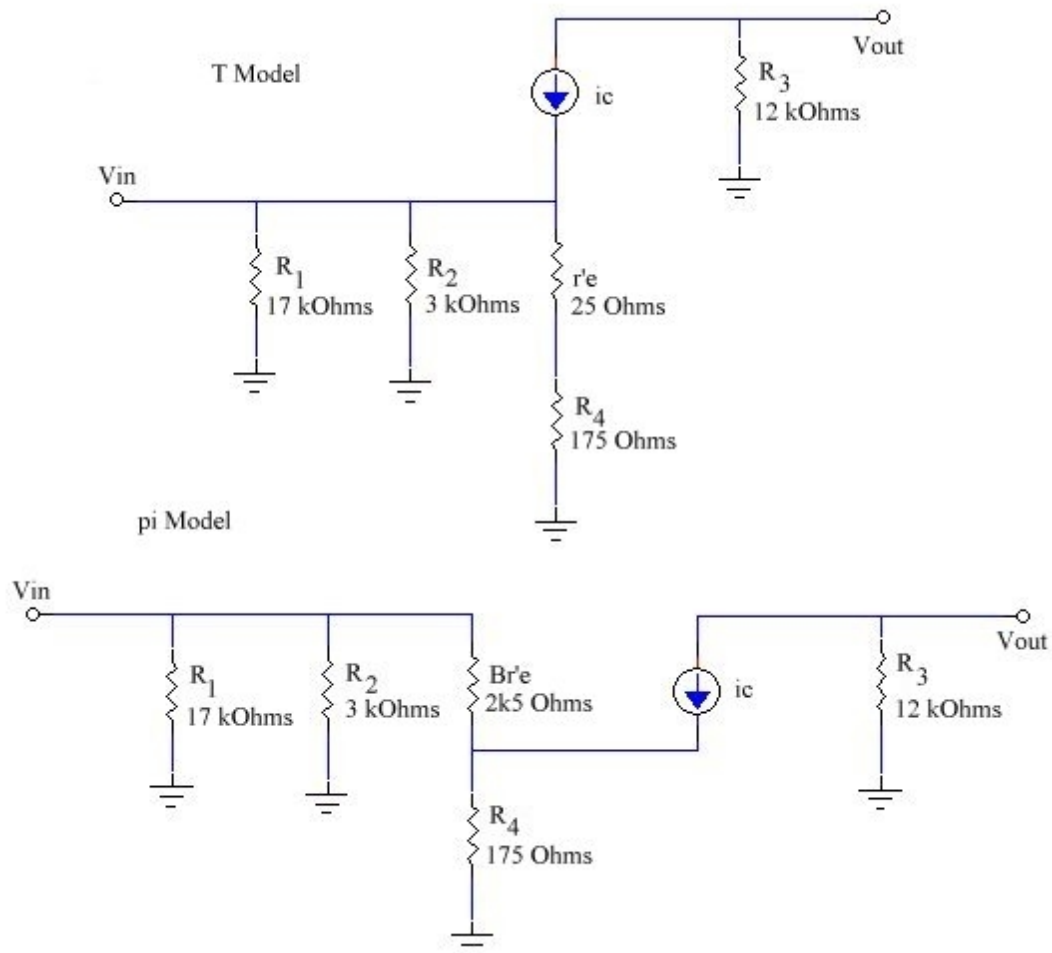$$A_V = \frac{-R_3}{r'e + R_4} = \frac{-12k\Omega}{25\Omega + 175\Omega} = -60$$

13

Question 6 Continued

c) Sketch the T and π transistor ac models for this circuit.
(Remember to label all components)

T Model

Vin

Vout

ic

R_3
12 kOhms

R_1
17 kOhms

R_2
3 kOhms

r'e
25 Ohms

R_4
175 Ohms

pi Model

Vin

Vout

R_1
17 kOhms

R_2
3 kOhms

Br'e
2k5 Ohms

ic

R_3
12 kOhms

R_4
175 Ohms

Question 6 Continued

d) Sketch the DC transistor model for this circuit.
(Remember to label all components)

DC Model

$V_{CC} = +20$ V

R₁ 17 kOhms

R₃ 12 kOhms

V_{BE}

I_C

R₂ 3 kOhms

R₄ 175 Ohms

R₅ 2k05 Ohms
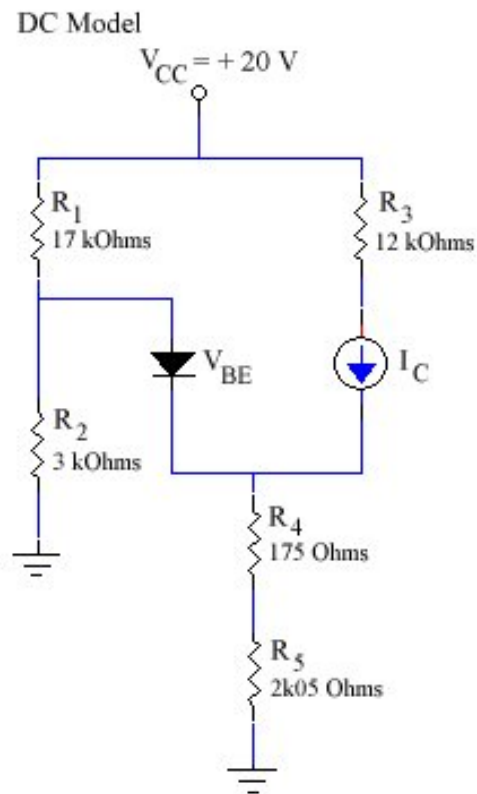
e) Is this a stiff voltage divider bias?
(You must show proof to support your answer)

$$R_1//R_2 = \frac{17k\Omega \times 3k\Omega}{17k\Omega + 3k\Omega} = 2.55k\Omega$$

$$R_E = R_4 + R_5 = 175\Omega + 2.05k\Omega = 2.225k\Omega$$

Definition of a stiff voltage divider bias is $R_1//R_2 < 0.01 \beta R_E$

Since $\beta = 100$ then $0.01 \beta = 1$ and   2.55 kΩ is **NOT** less than 2.225 kΩ

Therefore this is **NOT** a stiff voltage divider bias.